R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 4 lines 8-10, page 6 lines 9-11 and FIG. 2, as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-5 and 7-22 under 35 U.S.C. §102(b) as being anticipated by Fujimoto '710 has been obviated in part, is respectfully traversed in part, and should be withdrawn.

Fujimoto concerns a system and method for controlling a display of graphics data pixels on a video monitor having a different display aspect ratio than the pixel aspect ratio (Title). In contrast, claim 1 provides (i) a bus, (ii) a first data modification circuit configured to generate a first output data stream in response to performing a first modification on at least one first image from a first input data stream received from the bus and (iii) a composite circuit configured to generate a combined output data stream on the bus in response to performing a spatial combination of the first output data stream and a second output

data stream. In contrast, Fujimoto appears to be silent regarding a bus presenting graphics data (asserted similar to the claimed first input data stream) and receiving a signal generated by an alpha-blending circuit 108 (asserted similar to the claimed combined output data stream). Therefore, Fujimoto does not appear to expressly or inherently disclose (i) a bus, (ii) a first data modification circuit configured to generate a first output data stream in response to performing a first modification on at least one first image from a first input data stream received from the bus and (iii) a composite circuit configured to generate a combined output data stream on the bus in response to performing a spatial combination of the first output data stream and a second output data stream as presently claimed. As such, claim 1 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 11 provides steps for (A) reading a first input data stream of a plurality of data streams from a memory and (D) writing a combined output data stream to the memory. In contrast, Fujimoto appears to be silent regarding a memory from which graphics data (asserted similar to the claimed first input data stream) is read and to which a signal generated by the alpha-blending circuit 108 (asserted similar to the claimed combined output data stream) is written. Therefore, Fujimoto does not appear to expressly or inherently disclose steps for (A) reading a

first input data stream of a plurality of data streams from a memory and (D) writing a combined output data stream to the memory as presently claimed. Claim 22 provides language similar to claim 11. As such, claims 11 and 22 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 2 provides that an apparatus **forms** a block modify and move engine. In contrast, the Office Action appears to be treating the claim as "an apparatus **comprising** a block modify and move engine." In particular, no evidence or convincing line of reasoning is provided how circuits 104, 155 and 108 of Fujimoto (asserted similar to the claimed first data modification circuit and the claimed composite circuit) form a block modify and move engine. Therefore, *prima facie* anticipation has not been established. The Examiner is respectfully requested to either (i) clearly and concisely explain how the circuits 104, 155 and 108 of Fujimoto form a block modify and move engine or (ii) withdraw the rejection.

Claim 4 provides a first data modification circuit configured to covert an input format of a first input data stream and an output format of a first output data stream between a video data format and a graphics data format. In contrast, Fujimoto appears to be silent regarding either (i) a signal generated from a 1st scaler circuit 106 as having a video format or (ii) a signal received by a VRAM 103 as having a video format. Furthermore, the

Office Action fails to cite any text or figures of Fujimoto in arguing the rejection. Therefore, *prima facie* anticipation has not been established. Claim 14 provides language similar to claim 4. The Examiner is respectfully requested to either (i) clearly and concisely identify where Fujimoto expressly or inherently discloses converting between a video format and a graphics format or (ii) withdraw the rejections for claims 4 and 14.

Claim 5 provides a first output data stream comprising a plurality of video pictures. In contrast, Fujimoto appears to be silent regarding a signal generated by the 1st scaler circuit 106 (asserted similar to the claimed first output data stream) having a plurality of **video pictures**. Therefore, Fujimoto does not appear to expressly or inherently disclose a first output data stream comprising a plurality of video pictures as presently claimed.

Claim 5 further provides a second output data stream comprising graphics data. In contrast, Fujimoto appears to be silent regarding a signal generated by a 2nd scaler circuit 107 comprising **graphics data**. Therefore, Fujimoto does not appear to expressly or inherently disclose a second output data stream comprising graphics data as presently claimed. In general, the signals generated by the scaler circuits 106 and 107 of Fujimoto are backwards compared with the claimed signals. As such, claim 5 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 8 provides a first data modification circuit configured to perform separation of color components in each of a plurality of first images in a first data stream. In contrast, the Office Action provides no evidence or convincing line of reasoning that Fujimoto expressly or inherently discloses separation of color components by any of the circuits 104 and 155 (asserted similar to the claimed first data modification circuit). Furthermore, the "implied" argument presented in the Office Action is not an appropriate standard for a 35 U.S.C. §102 rejection. Therefore, *prima facie* anticipation has not been established. Claim 17 provides language similar to claim 8. The Examiner is respectfully requested to either (i) identify where the claim limitations are expressly disclosed in Fujimoto, (ii) explain why the claim limitations are inherent to Fujimoto and provide evidence of the inherency or (iii) withdraw the rejections for claims 8 and 17.

Claim 11 provides that a spatial combination (performed by a composite circuit) is a bitwise logical operation on a first output data stream and a second output data stream. In contrast, the Office Action fails to provide any evidence or convincing line of reasoning that the alpha-blending circuit 108 of Fujimoto (asserted similar to the claimed composite circuit) performs a bitwise logical operation as presently claimed. Furthermore, a Bit BLT circuit 202 of Fujimoto (asserted as performing the claimed bitwise logical operation) does not appear to be part of the alpha-

blending circuit 108. Therefore, Fujimoto does not appear to expressly or inherently disclose the structure of claim 11. As such claim 11 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 21 provides a memory configured to buffer a first data having a first format, a second data having a second format and a third data. In contrast, Fujimoto appears to be silent regarding a memory buffering the claimed first, second and third data. Furthermore, the "implied" argument presented in the Office Action is not a proper standard for a 35 U.S.C. §102 rejection. Still further, the Office Action improperly asserts that a display controller 155 of Fujimoto simultaneously anticipates both the claimed first data modification circuit and the claimed second expander circuit. Therefore, *prima facie* anticipation has not been established. The Examiner is respectfully requested to either (i) identify where Fujimoto expressly discloses a memory for buffering data as presently claimed, (ii) explain why a memory for buffering data is inherent to Fujimoto and provide evidence of the inherency or (iii) withdraw the rejection.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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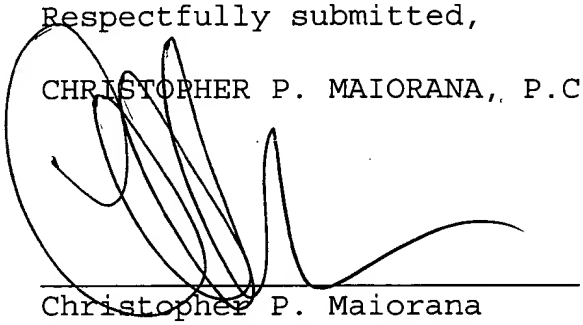

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